



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,849	02/04/2002	Sung-Kwon Lee	29926/38060	5173

4743 7590 08/05/2004

MARSHALL, GERSTEIN & BORUN LLP  
6300 SEARS TOWER  
233 S. WACKER DRIVE  
CHICAGO, IL 60606

EXAMINER

RUGGLES, JOHN S

ART UNIT PAPER NUMBER

1756

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/066,849

Applicant(s)

LEE ET AL.

Examiner

John Ruggles

Art Unit

1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4-14 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 June 2004 has been entered.

Claims 1-2, 4, and 6-7 have been currently amended; claims 3 and 15-20 remain as previously canceled; claims 5 and 13-14 remain as originally filed; and claims 8-12 remain as previously presented. Therefore, only claims 1-2 and 4-14 remain under consideration.

### ***Specification***

The previous objections to the abstract of the disclosure have been overcome by the currently amended abstract, in accordance with suggestions previously made by the examiner.

While further amendments to the specification have again overcome the previously exemplified objections thereto as well as several more not previously exemplified, examples of those still remaining and/or introduced by current amendments to the specification are set forth below.

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is still replete with terms, which are not clear,

Art Unit: 1756

concise and exact. The specification should again be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some remaining unclear, inexact or verbose terms used in the specification are: (1) in line 2 of the amendment to the paragraph beginning at page 1 line 17 of the original specification (found at the top of page 2 in the amendment filed 17 June 2004), “self-align dual damascene process” should have been --self-aligned dual damascene process--, to be grammatically correct (this same objection also applies to at least lines 1 and 3 of the amendment to the paragraph beginning at page 1 line 20 of the original specification and in line 6 of this amended paragraph, “portion of conductive layer” should have been --portion of the conductive layer-- to more clearly state that this conductive layer is the same as that described in the previous sentence, just as found in the earlier version of this paragraph as originally filed); (2) Applicants must show specific support in the specification as originally filed for their current addition of the phrase “or intact” between “remaining” and “etching stop layer” in line 4 of the amendment to the paragraph beginning at page 4 line 10 in the original specification (or delete this new phrase if it constitutes new matter); (3) on page 3 of their most recent submission, Applicants have apparently replaced the wrong paragraph beginning at page 5 line 5 of the original specification with an amended version of the *previous* original specification paragraph beginning at page 5 line 2 to correct the misspelling of “aherein” to --wherein-- in line 4 (even though replacement of the wrong paragraph is believed to have been inadvertent, Applicants must still resubmit corrected versions of **both** the paragraph beginning at page 5 line 2 to correct the misspelling remaining in line 4 and the following paragraph beginning at page 5 line 5 to reinstate the brief description of Figures 1A to 1D); (4) in the amendment to the paragraph beginning at page 5 line 27 of the original specification, the previous phrase “selectively etched

Art Unit: 1756

to exposure a part” has been changed to “selectively etched to expose a part via or trench”, but this raises another question of possible new matter (unless Applicants can point to specific support for this substitution in the original specification) and even makes unclear the antecedent basis for the phrase “the exposed part” remaining at page 6 line 2 of the original specification; (5) at least the amendment to the paragraph beginning at page 6 line 32 is non-compliant because Applicants have failed to mark the addition of “(Fig. 3B)” by underlining after “the via hole 39” in line 4 as required by 37 CFR 1.121 as amended and published on 30 June 2003 in the Federal Register (68 Fed. Reg. 38611), a copy of which is attached to this Office action (in response, Applicants must resubmit all previous non-compliant section(s) in full compliance with this statute); (6) in the amendment to the paragraph beginning at page 7 line 8 in the original specification, “where where it can be used to form” is repetitive and should be corrected to -- where it can be used to form-- in line 4, and in this same amended paragraph at line 7, Applicants must also clarify the meaning of “nitrogen layer” (e.g., whether or not --nitride layer-- was intended, etc.); and (7) in line 2 of the amendment to the paragraph beginning at page 9 line 6 [rather than line 5] of the original specification, “trench 39 (see Figs. 3C-3E)” should have been changed to --via hole 39 (see Figs. 3B-3E)--, in order to better correlate with these drawings.

While a more extensive list of examples has been given in this Office action than in previous Office actions, Applicants are again reminded that due to the large number of errors, those listed here are merely examples of the corrections needed and do not represent an exhaustive list thereof.

Appropriate correction is again required. An amendment filed making all appropriate corrections must be accompanied by a statement that the amendment contains no new matter and

Art Unit: 1756

also by a brief description specifically pointing out which portion of the original specification provides support for each of these corrections.

### ***Claim Objections***

While amendments have overcome the previous specific objections to the claims, another such objection is set forth below.

Claim 7 is objected to because of the following informalities: in lines 2-3 of claim 7, “any one selected from the group consisting of an USG layer deposited by a high density plasma, an oxide deposited by” should be changed to --any one selected from the group consisting of an USG layer deposited by a high density plasma and an oxide deposited by either--, in order to be grammatically correct--. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

While current amendments to the claims have overcome the previous rejection of claims 1-14 under the second paragraph of 35 U.S.C. 112, these amendments have also necessitated a new rejection under the first paragraph of 35 U.S.C. 112 as set forth below.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not

Art Unit: 1756

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the currently amended version of claim 6, a void is now recited to be formed “in the fourth interlayer insulating layer”, rather than the void being formed in the via hole (as was previously recited in claim 6). Page 7 lines 21-28 of the original specification describe formation of the fourth interlayer insulating layer “in order to form a void (B) is formed in the via hole 39” (page 7 lines 27-28). While this original disclosure supports forming a void within the via hole, it does not clearly specify that such a void was intended to be formed within the fourth interlayer insulating layer. Applicants must either show clear support in the specification as originally filed for this new language in claim 6 or delete this language as new matter. Claims 7-8 depend on claim 6.

Nevertheless, claims 6-8, as currently amended, are still treated on the merits (for the reasons set forth below).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 4-5, and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent 6,093,632) in view of Lin, et al. (US Patent 6,042,999) and further in view of Yeh, et al. (US Patent 6,180,514).

Lin '632 teaches a modified dual damascene method for manufacturing multi-level interconnection lines in a semiconductor device. The method involves forming conductive (copper, Cu, instant claim 13) interconnection lines 2 in a first (1<sup>st</sup>) insulator (silicon oxide) 1, which is understood to be on a semiconductor substrate. Layers 1 and 2 are covered by a 1<sup>st</sup> etching stop layer 3 (silicon nitride, instant claim 3), a second (2<sup>nd</sup>) insulator (silicon oxide) 4 formed by either plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD) to 4,000-15,000 Å thick (column 4, lines 6-9, instant claims 9-10), and a 2<sup>nd</sup> etching stop layer 10a (silicon nitride 200-2,000 Å thick by e.g., PECVD, etc., column 5, lines 25-27, instant claims 11-12), as shown in Figure 4 (column 5, lines 18-28). A resist pattern 11 is used as an etching mask to pattern narrow openings 12a for via holes in the 2<sup>nd</sup> etching stop layer 10a, to form a patterned etching stop layer 10b, as shown in Figure 5 (column 5, lines 29-43). After removing the resist, the patterned etching stop layer 10b is covered by a third (3<sup>rd</sup>) insulator layer 13 (silicon oxide by e.g. PECVD, etc. to about 3,000-15,000 Å thick), followed by forming another patterned resist mask 14, having wider openings 15a for forming wide trenches connecting over the narrow via holes, as shown in Figure 6 (column 5, lines 43-53, instant claim 5). The wide trenches and narrow via holes are etched through the resist mask 14 and etching stop pattern portions 10b through the insulators 13 and 4 and etching stop layers 10b and 3 down to the conductive interconnection lines 2, as shown in Figure 7 (column 5, line 54 to column 6, line 8, instant claim 4). A conductive layer 16 is

Art Unit: 1756

formed to fill the trenches and connected underlying via holes onto the tops of conductive lines 2, as shown in Figure 8 (column 6, lines 9-29, instant claims 1-2). While not specifying the thickness of the Cu conductive interconnection lines 2, the figures suggest this thickness is similar to those of insulator layers 3 and 13 (or about 3,000-15,000 Å thick, instant claim 14). Lin '632 patterns the etching stop layer to leave only small area islands 10b, in order to reduce or limit increase in capacitance usually caused by wider area etching stop layers (column 2, lines 15-25). Also, while the teachings of Lin '632 are described in terms of this method as a preferred embodiment, it is understood by those skilled in the art of dual damascene multi-level interconnection manufacture of semiconductor devices that various changes may be made in the details of this embodiment without departing from the spirit and scope of these teachings (column 6, lines 36-40).

While teaching a dual damascene method for manufacturing multi-level interconnection lines similar to the instant invention, Lin '632 does not specify [1] forming the via holes before forming the patterned etching stop patterns around the via inlets and subsequent trench patterning of the overlying 3<sup>rd</sup> insulator layer; nor [2] forming the conductive layer in the trench and via hole to at least partially cover the remaining narrow portions of the upper 2<sup>nd</sup> etching stop layer.

Lin '999 shows a robust dual damascene method of manufacturing multi-level interconnection lines in a semiconductor device that involves formation of a via 145, before forming an overlying trench 165, as shown in Figures 2b and 2f (column 5, line 20 to column 6, line 18, for [1] forming the via holes before forming the patterned etching stop patterns around the via inlets and subsequent trench patterning of the overlying 3<sup>rd</sup> insulator layer).

Yeh discloses a dual damascene process for forming a conductive interconnect 218 over barrier layer 217 in a trench and connected underlying via hole in which the conductive metal layer 218 at least partially covers remaining portions of an etching stop pattern 214 of tantalum nitride positioned around the via hole inlet as shown in Figures 2F-2H (title, column 4 lines 6-36, for [2] forming the conductive layer in the trench and via hole to at least partially cover the remaining narrow portions of the upper 2<sup>nd</sup> etching stop layer). Like Lin '632, Yeh also decreases the horizontal dimension of the etch stop pattern 214 remaining in the interconnect structure. The dual damascene process is improved with resulting reduced RC delay for achieving higher performance in integrated circuits (column 2 lines 1-3 and column 4 lines 37-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have changed the order of steps in the embodiment described by Lin '632 so as to form via openings before forming the patterned etching stop layer portions 10b, then overlying and patterning the 3<sup>rd</sup> insulator layer to form trenches therein. This is because Lin '632 suggests changes to the details of his preferred embodiment without departing from the spirit and scope of those teachings relating to use of patterned reduced area islands of etching stop material to reduce capacitance under that which would have resulted if a wider area etching stop layer had been used. Also, formation of via holes followed by subsequent formation of trenches over these via holes (via first, rather than trench first) was already known in dual damascene semiconductor device manufacture at the time of the instant invention, as shown by Lin '999 [1]. It would also have been obvious to modify the dual damascene process taught by Lin '632 and shown by Lin '999 by forming the conductive layer in the trench and via hole to at least partially cover the

Art Unit: 1756

remaining narrow portions of the upper 2<sup>nd</sup> etching stop layer as disclosed by Yeh. This is because Yeh, like Lin '632, also decreases the horizontal dimension of the etch stop pattern remaining in the interconnect structure in order to improve the dual damascene process with resulting reduced RC delay for achieving higher performance in integrated circuits.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin '632 in view of Lin '999, further in view of Yeh, and further in view of Akahori, et al. (US Patent 6,737,350).

While teaching other aspects of the instant invention, neither Lin '632, Lin '999, nor Yeh specifically teach forming a void within the fourth interlayer insulating layer over the via hole.

Akahori describes a dual damascene method for manufacturing a semiconductor device that seeks to reduce the dielectric constant of an interlayer dielectric film used therein in order to accelerate operation of the resulting overall device (column 1 lines 26-30). Various interlayer dielectric film materials have been considered to replace SiO<sub>2</sub> (having a dielectric constant of about 4) as having suitably lower dielectric constants (e.g., 3.5 for SiOF, even lower for CF, etc., column 1 lines 30-37). The method includes formation of a top dielectric film (4 or 111) deposited over a previously formed via hole 31 in a lower dielectric layer 3 (e.g., SiO<sub>2</sub>, etc.), which can either be formed (1) directly on a silicon substrate in the lowest layer of a semiconductor device having a multilayer metallization structure or (2) even in an upper wiring layer thereof (column 3 line 54 to column 4 line 3). The top dielectric film (4 or 111) is deposited so as to project inwardly from the periphery of the via hole 31, without embedding top dielectric film material in the via hole 31 (Figures 7 (a) and 11 (a), column 5 lines 50-55). Thus,

Art Unit: 1756

this top dielectric film (4 or 111) is considered to be analogous to the instant fourth interlayer insulating layer "41" shown by instant Figure 3D and has an intermediate curved profile shaped very much like that of area "B" in the instant fourth interlayer insulating layer "41". Akahori describes a simple technique for making a semiconductor device having a complicated dual damascene shape to improve throughput and reduce manufacturing costs (column 7 lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a lower dielectric constant top dielectric film or fourth interlayer insulating layer deposited to form an intermediate shape having a void therein as described by Akahori in the dual damascene method taught by Lin '632, shown by Lin '999, and disclosed by Yeh in order to avoid embedding of top dielectric or fourth interlayer insulating layer material in the underlying via hole and also to reduce the overall dielectric constant of the interlayer dielectric film for accelerating operation of the resulting overall device. It is also noted that (1) all four references relate to the same art of dual damascene manufacture of multi-level interconnects in semiconductor devices and (2) at least Lin '632, Yeh, and Akahori further share a common interest in reducing the overall dielectric constant in such semiconductor devices (which is understood to reduce parasitic capacitance and device delay to accelerate overall device performance).

### ***Response to Arguments***

Applicant's arguments with respect to the claims filed on 17 June 2004 have been considered but are moot in view of the new ground(s) of objection and rejection that have been set forth above.

The previous objections to the abstract of the disclosure have been overcome by the currently amended abstract.

While further amendments to the specification have again overcome the previously exemplified objections thereto as well as several more not previously exemplified, more extensive examples of those still remaining and/or introduced by current amendments to the specification have been set forth above.

While amendments have overcome most of the previous objections to the claims, another such objection has been set forth above.

While current amendments to the claims have overcome the previous rejection of claims 1-14 under the second paragraph of 35 U.S.C. 112, another new rejection under the first paragraph of 35 U.S.C. 112 has been set forth above, as necessitated by these amendments.

Instant claims 1-2 and 4-14, even as currently amended, have been considered to be obvious over the newly combined prior art for at least the reasons cited above.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 571-272-1390. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 1756

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John Ruggles  
Examiner  
Art Unit 1756



MARK F. HUFF  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 1700